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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/749,130

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Alessia Pavan

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996 7590 06/06/2007  
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EXAMINER
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FARAHANI, DANA

ART UNIT	PAPER NUMBER
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2891

MAIL DATE	DELIVERY MODE
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06/06/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/749,130

Applicant(s)

PAVAN ET AL.

Examiner

Dana Farahani

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6, 15-26 and 31-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 15-26 and 31-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2007 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                        | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations, that of said floating gate insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

*Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-6, 15-26 and 31-38 are rejected under 35 U.S.C. 103(a) as being unpatentable Baker et al., hereinafter Baker (US Patent 4,852,062) in view of Catabay et al., hereinafter Catabay (US Patent 6,800,940), both previously cited.

Regarding claims 1, 4, 5 and 6, Baker discloses in figure 11, a memory comprising:

a floating gate transistor including a source regions and drain regions, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region 52 and a control gate region 54, characterized in that said floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source and drain regions, by a dielectric layer 60, 64 with a dielectric constant value.

Baker does not disclose the dielectric constant value is between 1 and 3.9 (low dielectric), and the layer is formed by an oxide layer, hydrated with alkylic groups.

Catabay discloses in figure 4, and column 6, lines 23-37, a carbon doped silicon layer 30 in the integrated circuit structure shown. Catabay further discloses this kind of layer is void free and have a dielectric constant of less than 3 (see column 4, lines 35-40 and 52-55), further disclosing low dielectric constant values reduces horizontal capacitance between conductive lines (see column 2, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in

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the art at the time of the invention to use carbon doped oxide layer in the structure of Baker to benefit from the advantageous properties of the layer such as reduced capacitance between the gate electrodes. Note that using alkylic groups to dope the oxide layer is a method of doping the oxide layer.

Regarding claim 2, the floating gate regions are covered by a dielectric layer 58 before being insulated from each other through said dielectric layer with low dielectric constant value.

Regarding claim 3, the dielectric layer with low dielectric constant value is bounded between said floating gate regions, as can be seen in figure 11.

Regarding claims 15-26, Baker in view of Catabay renders obvious the limitations in the claims, as discussed above, further disclosing the cells are organized in a matrix form, see figure 1A; a word line shown in the same figure; where adjacent cells are connected to the same word line (see fig. 1A). Thus, the control gate regions are electrically connected.

Regarding claims 31-34, dielectric regions 56 are in direct contact to the floating gates, and the motivation as to making them low dielectric is stated above. Also, a second dielectric 66 is formed on the first dielectric region.

Re. claims 35-38, if the dielectric layers 24a and 30 of the Catabay reference are incorporated in the Baker reference, then the resulting device would have a dielectric layer completely filling a space between adjacent memory cells coupled to the same word line (fig. 1A of the Baker reference).

*Response to Arguments*

4. Applicants' arguments with respect to claims have been considered but are not persuasive.

Applicants argue that in the Baker reference insulators 60 and 64 of figure 11 do not insulate the two floating gates 52 laterally but instead insulate the gates in direction parallel to the plane containing the gate, source and the drain.

This argument is not persuasive. In the Baker reference, the aforementioned two insulators insulate the cells both along the bit line, horizontally and along the word line, as defined in applicants' response. This is because although the insulators shown in the figure are from a cross sectional perspective, the insulator surely extends in three directions: laterally, i.e., along an axis extending from source to drain; the insulators clearly have height; and they extend along the direction of an axis which is orthogonal to a plane containing the gate, source and the drain. That is, the insulating film composed of the two aforesaid insulators must have a width, which is along the axis of the orthogonal line.

*Conclusion*

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DF

  
**B. WILLIAM BAUMEISTER**  
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